MEMORY DEVICE CAPABLE OF SUPPORT-ING SEQUENTIAL MULTIPLE-BYTE READ-ING

Abstract

When the memory device receives address information and byte information M, the memory device continuously provides M bytes corresponding to M addresses following an address assigned in the address information. The memory device includes: an address calculation module, an address buffer, a decoding module, a plurality of memory units and output buffers. Each output buffer is capable of receiving data of two units and sequentially outputting the data. When the address calculation module stores an address in the address buffer, the decoding module makes cells corresponding to the address simultaneously output data to the output buffers, such that the output buffers sequentially output data of respective unit. The address calculation module starts to count the next address, such that when the output buffer finishes outputting, the next address is already stored in the address buffer, and the decoding module has already made units corresponding to the next address output data.